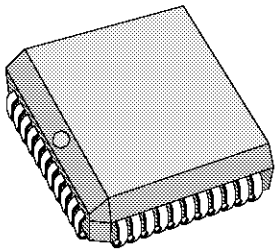
SGS-THOMSON MICROELECTRONICS

M62486R

VERY FAST CMOS 32K x 9 CACHE BRAM

ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIME 15ns
- FAST ACCESS TIMES: 8, 9ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- DUAL CHIP SELECTS for EASY DEPTH EXPANSION
- OUTPUT REGISTERS for PIPE-LINE READ BURSTS



PLCC44 (Q)

DESCRIPTION

The M62486R BRAM™ is a 288K (294,912 bit) CMOS Burst SRAM, organized as 32,768 words x

Figure 1. Logic Diagram

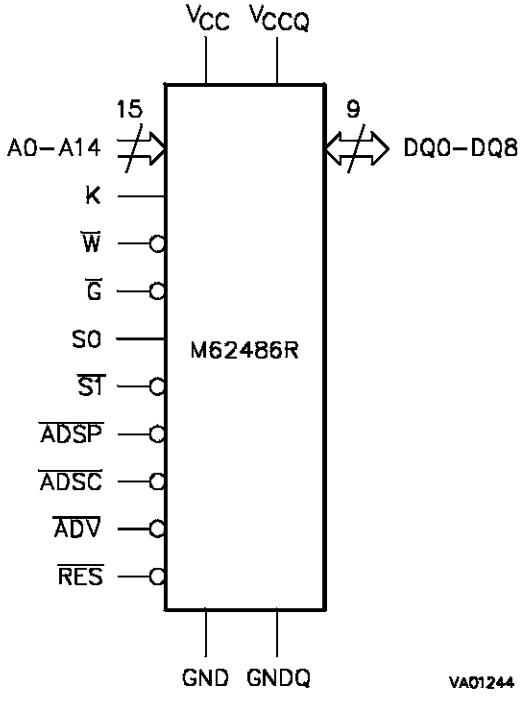


Table 1. Signal Names

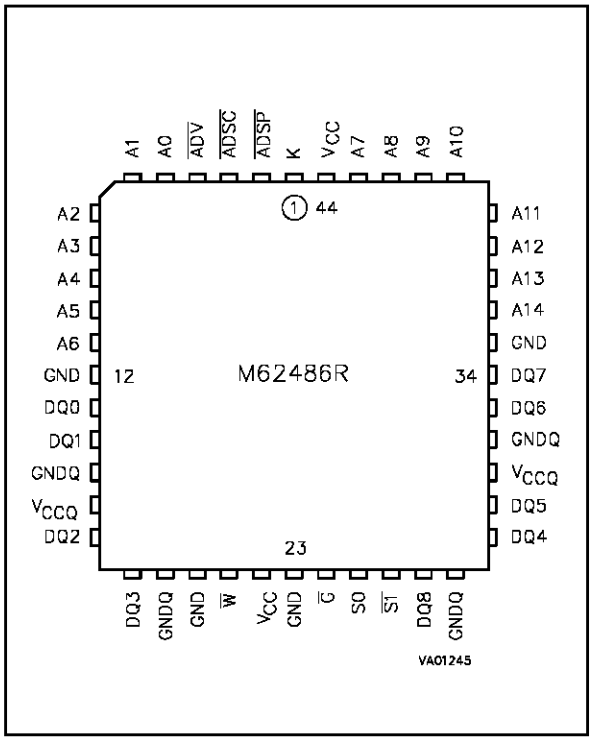
A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select 0, Active High
$\overline{S1}$	Chip Select 1, Active Low
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Cache Controller
$\overline{ADV}$	Burst Address Advance
V_{CC}	Supply Voltage
GND	Ground
V_{CCQ}	Supply Voltage (DQ)
GND_Q	Ground (DQ)

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1.2	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip.

The synchronous design provides precise control using an external clock (K) input. The M62486R is specifically adapted to provide a burstable, high performance secondary cache for the i486® microprocessor. The M62486R is available in a 44 lead Plastic Leaded Chip Carrier package (PLCC). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for DQ0-DQ8 to allow output levels referenced to 5V or 3.3V. For proper operation all GND and GND_Q pin must be connected to ground. $V_{CC} \geq V_{CCQ}$ at all times including power-up.

The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATIONS

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$), are clock controlled inputs through non-inverting, pos-itive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{ADV}$ input (burst address advance) provides control of the burst sequence, which imitates the i486 cache burst address sequence. Once a cache burst cycle begins, the subsequent burst address is generated internally each time the $\overline{ADV}$ input is asserted at the rising edge of the clock (K) input.

Table 3. Asynchronous Truth Table

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write(2)	X	Data In (High-Z)
Deselect	X	High-Z

Notes: 1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

Table 4. Burst Count Sequence

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	$\overline{A0}$
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	$\overline{A1}$	$\overline{A0}$

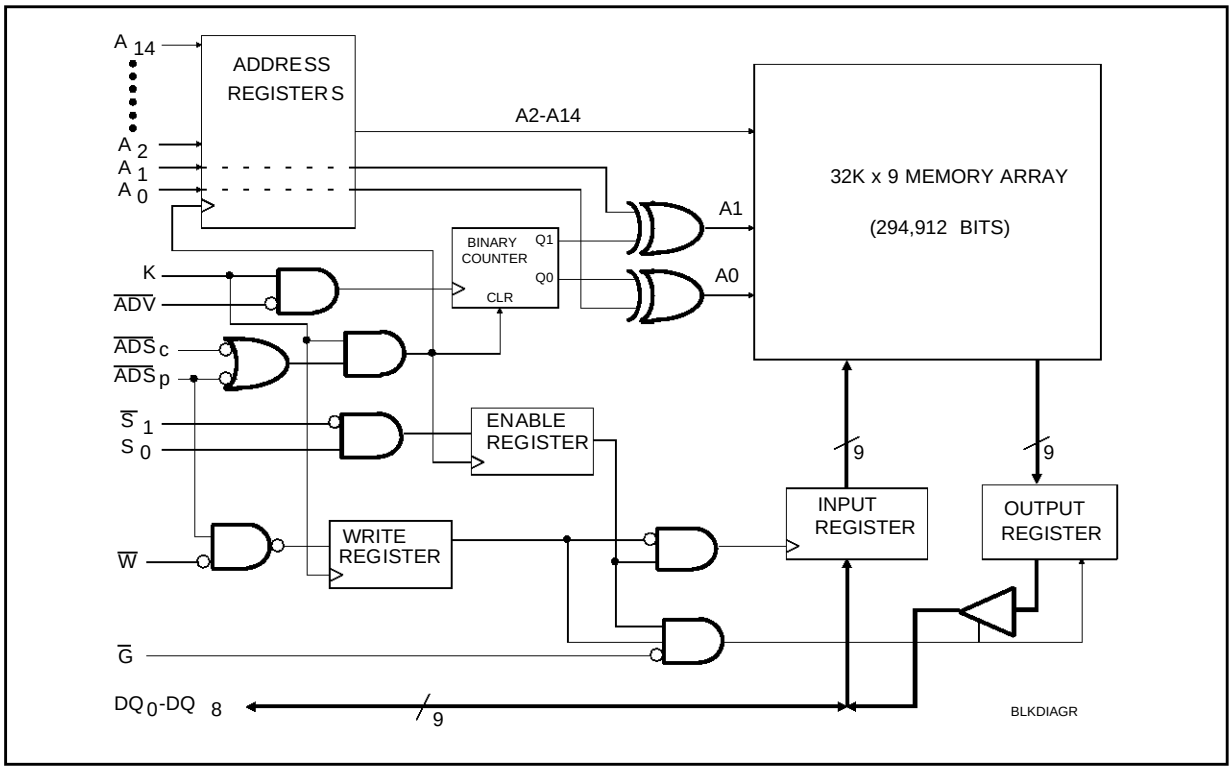
Note: The burst count sequence wraps around to the initial address after a full count is completed.

Table 5. Synchronous Truth Table

S0	$\overline{S1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Begin Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Begin Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Read Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst • Address	Read Cycle - Suspend Burst Sequence

Notes: 1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{ADSP}$ or $\overline{ADSC}$ is asserted for the device to remain enabled; Chip Selects are registered whenever ADSP or ADSC is asserted low at the rising edge of the clock.

Figure 3. Block Diagram



DEVICE OPERATIONS (cont'd)

The burst counter operates in the same manner for either cache burst write or read cycles. The $\overline{ADSP}$ and the $\overline{ADSC}$ inputs control the start and the duration of the burst sequence respectively. Each time either address status input is asserted low, a new external base address is registered on the positive going edge of the clock (K).

When $\overline{ADSP}$ is asserted low, any ongoing burst cycle is interrupted, and a read operation (independent of $\overline{W}$ and $\overline{ADSC}$) is performed at the new registered external base address. A new burst cycle is initiated each time $\overline{ADSP}$ is asserted. By asserting $\overline{ADSC}$ low, the present burst cycle (initiated by $\overline{ADSP}$) is interrupted and an extended burst read or write (depending upon the logic state of $\overline{W}$ at the rising edge of K) is performed at the new registered base address. Chip selects (S0 and $\overline{S1}$) are only sampled when a new base address is loaded. Therefore, the chip selects are registered when either address status input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either $\overline{ADSP}$ or $\overline{ADSC}$. The M62486R Truth Tables and timing diagrams reference specific device operations.

It should be noted that the M62486R allows a non-burst mode of operation where $\overline{ADSP}$ is the ADS# of the i486 processor in a 2-2 cycle mode of

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

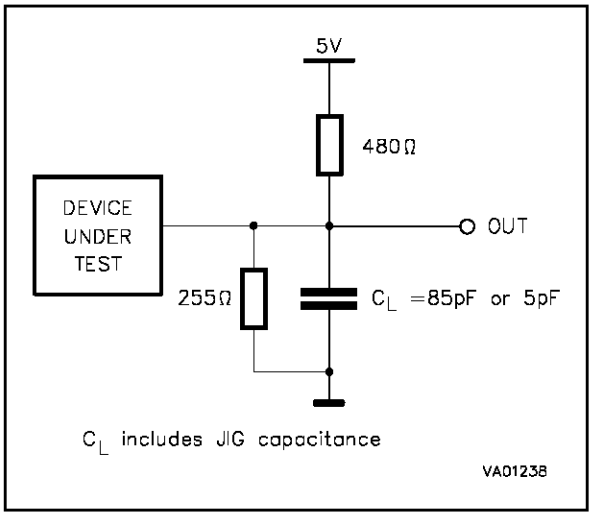


Table 6. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		10	pF

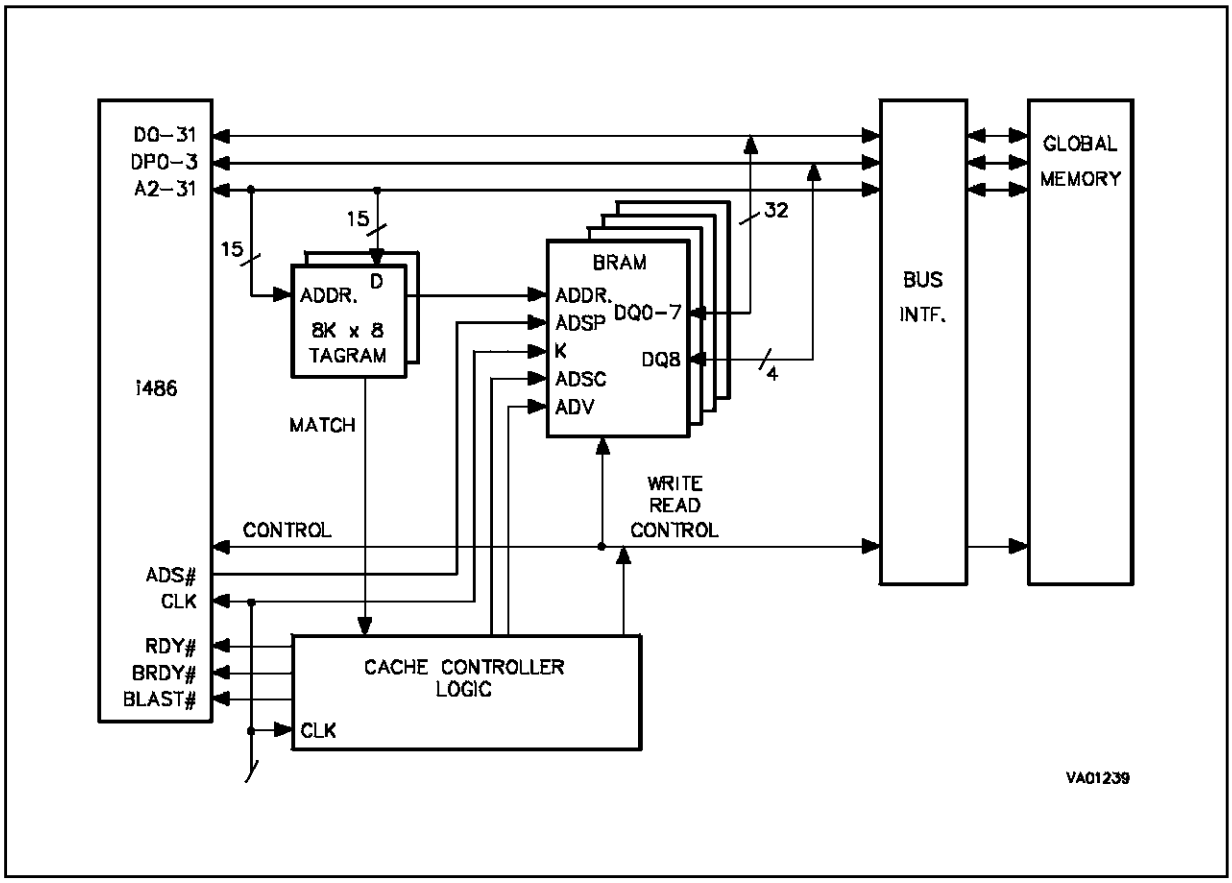
Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 7. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC1} [1]	Supply Current	$\overline{G}$ = V_{IH}, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All inputs = V_{IL} = 0V and V_{IH} ≥ 3V		180	mA
I_{CC2} [2]	Supply Current (Standby) TTL	S0 = V_{IL}, $\overline{S1}$ = V_{IH}		40	mA
I_{CC3} [3]	Supply Current (Standby) CMOS	S0 ≤ 0.2V, $\overline{S1}$ ≥ V_{CC} –0.2V		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{KHKH} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

Figure 5. General 128K Byte Cache Block Diagram



DEVICE OPERATIONS (cont'd)

operation, and $\overline{\text{ADSC}}$ is held high during T2 (see Figure 5). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input. Self-timed write cycles eliminate complex off-chip write pulse generation providing more flexibility for incoming signals.

The $\overline{\text{ADV}}$ input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time $\overline{\text{ADV}}$ is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced before the operation. Wait states can be inserted during burst cycles by holding the $\overline{\text{ADV}}$ pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

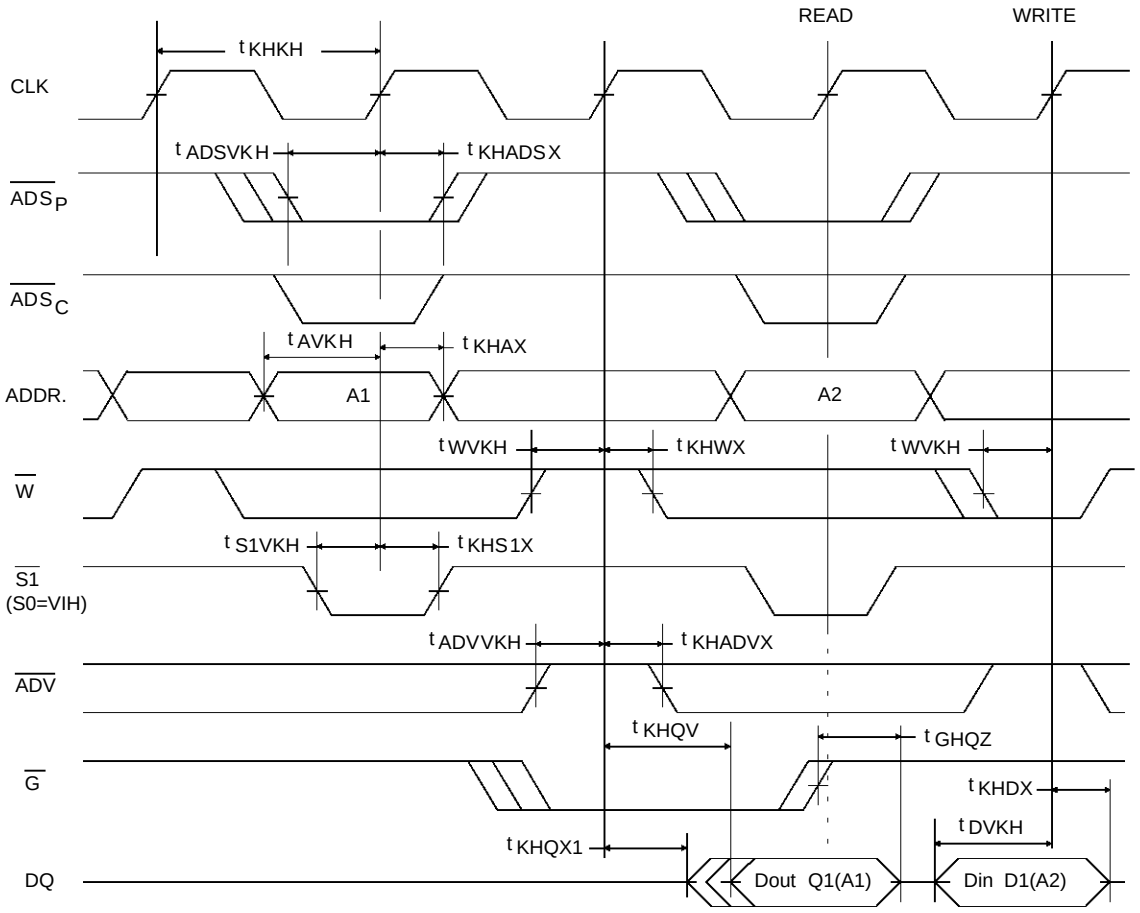
The M62486R is organized using the ninth bit as the parity bit to support byte parity. Since the i486 processor provides on-board parity generation and checking, the ninth bit of the cache Burst SRAM can be passed to one of the DP0-DP3 pins of the microprocessor. Thus the M62486R provides an architecture for building a 32K x 32bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Table 8. Read and Write Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	M62486R				Unit	Note
		8		9			
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	15		15		ns	
t_{KHQV}	Clock Access Time		8		9	ns	1
t_{KHKL}	Clock High Pulse Width	5.5		5.5		ns	
t_{KLKH}	Clock Low Pulse Width	5.5		5.5		ns	
t_{GLQV}	Output Enable Access Time		5		6	ns	1
t_{KHQX2}	Clock High to Output Hold Time	2		2		ns	1
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQX1}	Clock High to Q Active (Low-Z)	3		3		ns	2
t_{KHQZ}	Clock High to Q High-Z		6		6	ns	2
t_{GHQZ}	Output Disable to Q High-Z		6		6	ns	2
t_{AVKH}	Address Set-up Time	2		2		ns	3
t_{ADSVKH}	Address Status Set-up Time	2		2		ns	3
t_{DVKH}	Data In Set-up Time	2		2		ns	3
t_{WVKH}	Write/Read Set-up Time	2		2		ns	3
t_{ADVVKH}	Address Advance Set-up Time	2		2		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	2		2		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	2		2		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHADSX}	Address Status Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHADVX}	Address Advance Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes: 1. C_L = 85pF (see Figure 4).
2. Transition is measured ± 500 mV from steady-stage voltage with C_L = 5pF (see Figure 4). This parameter is sampled and not 100 % tested.
3. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

Figure 6. Non-Burst Read/Write Cycles



Note : Non-Burst Bus Cycle

K486R02

Figure 7. Burst Read Cycle

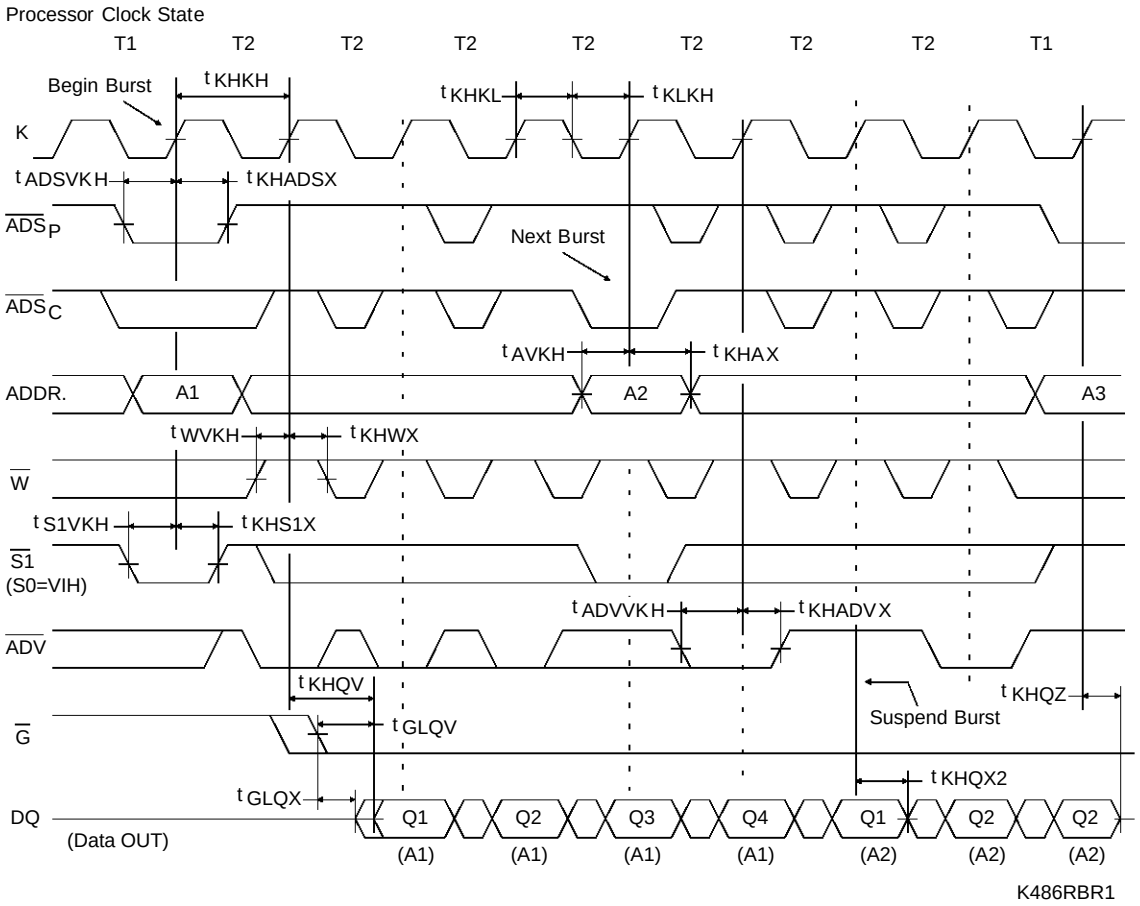


Figure 8. Burst Write Cycle

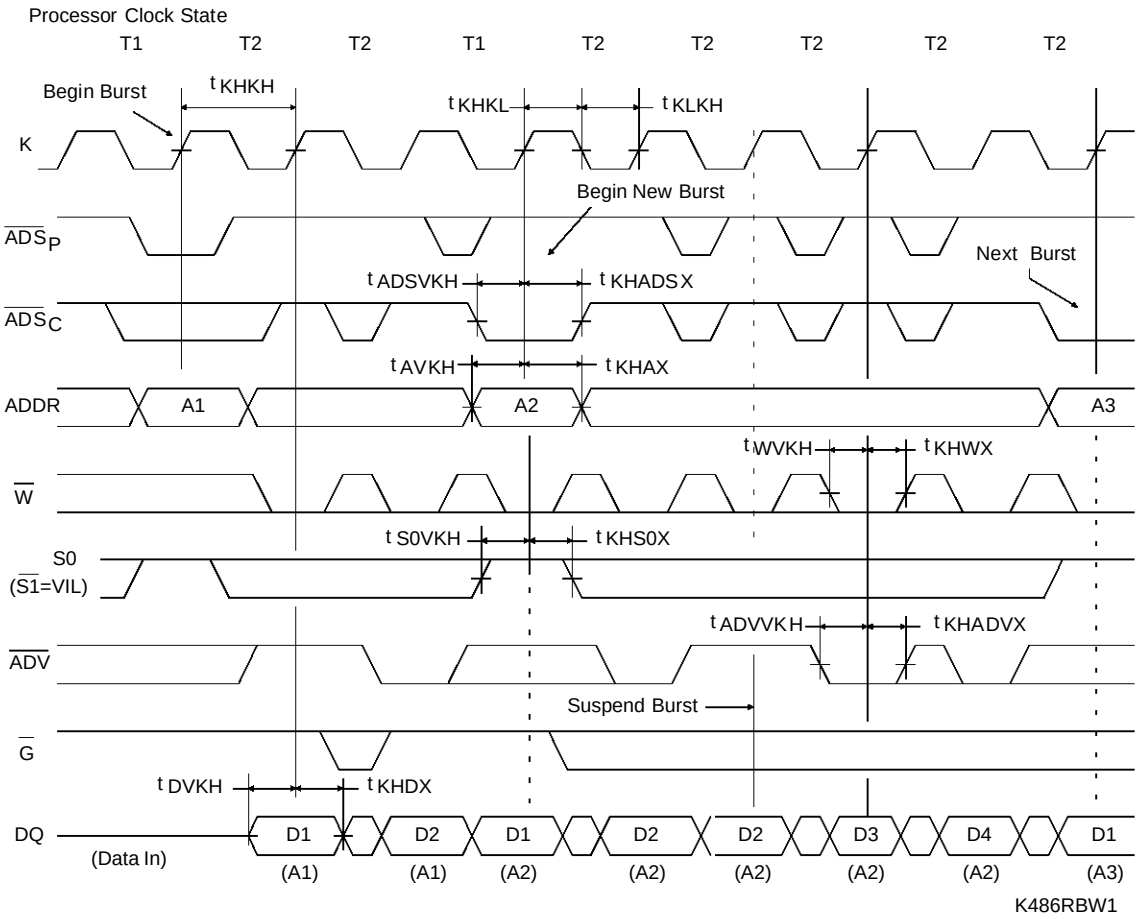
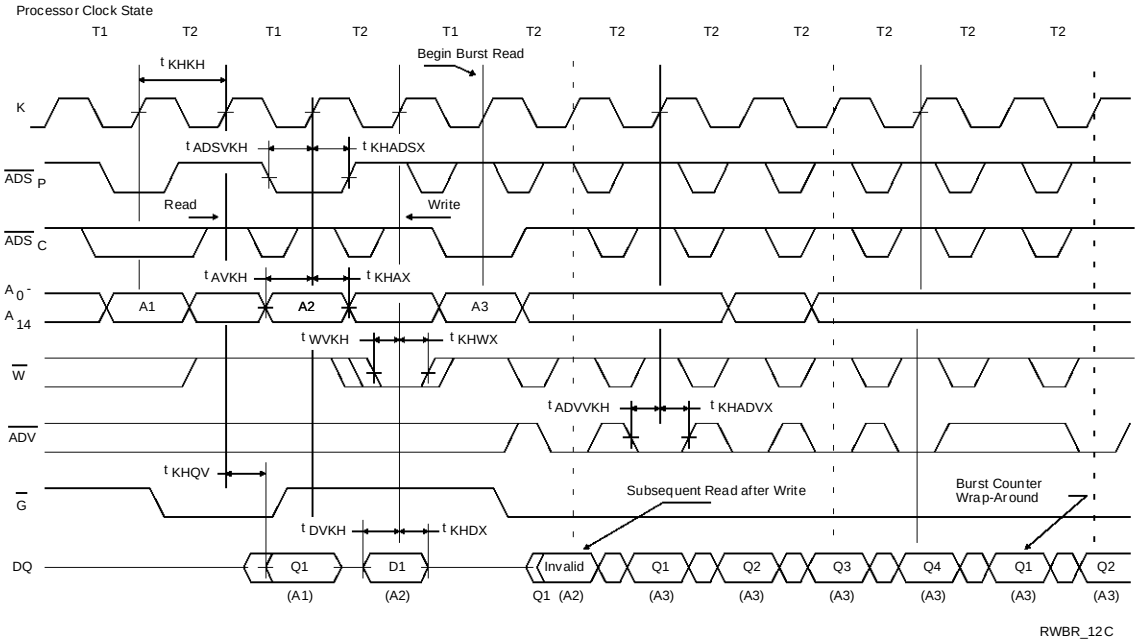
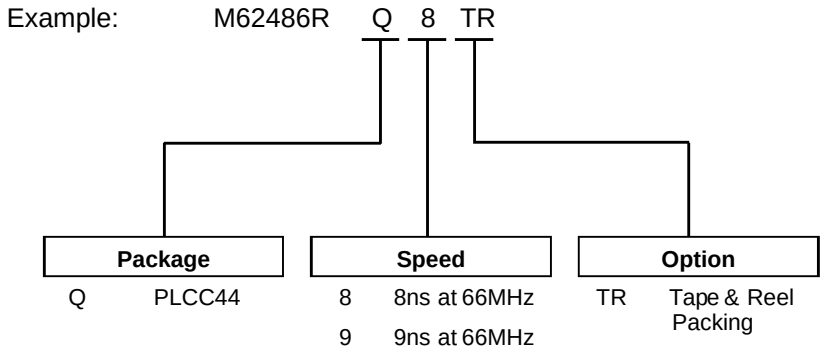


Figure 9. Combined Burst Read/Write Cycle



ORDERING INFORMATION SCHEME



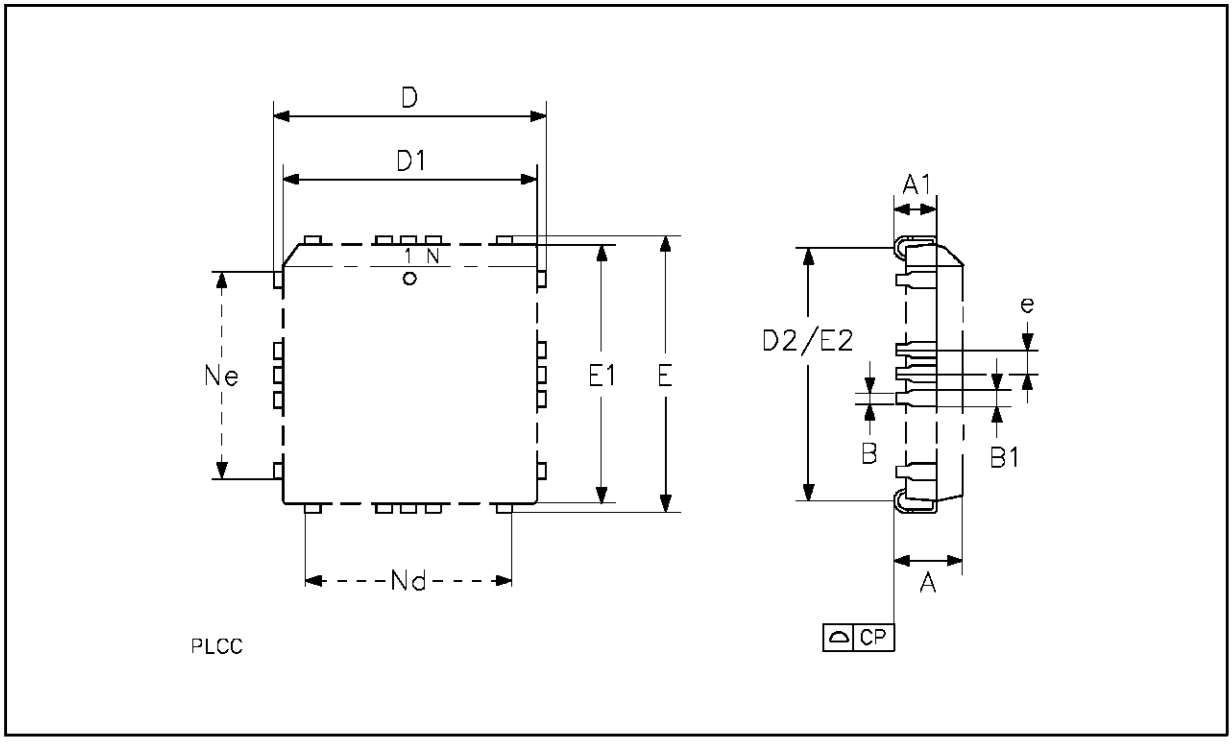
For a list of available options (Package, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
N	44			44		
CP			0.10			0.004

PLCC44



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